Final Project Report

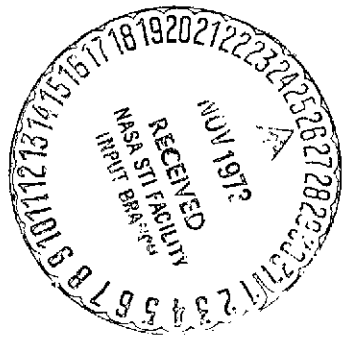
DEVELOPMENT OF A RUGGEDIZED 20-WATT, 2.3-GIGAHERTZ TRANSISTOR

10 November 1971 To 31 January 1973

Contract No. NAS 5-21668

Prepared by

RCA Solid State Division
Somerville, New Jersey



for

Goddard Space Flight Center
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ABSTRACT

The objective of this program was to develop a ruggedized transistor capable of meeting the following CW objectives at 2.3 gigahertz: a power output of 20 watts, a power gain of 6 dB, and an efficiency of 40 percent. Devices developed under this contract produced the following CW performance at 2.3 gigahertz: a power output of 23 watts, a power gain of 7.7 dB, and an efficiency of 40.0 percent. This performance was achieved with an eight-cell TA8407 transistor design having the following modifications: a thin pellet, high-frequency diffusion, high-level emitter ballasting, an optimized emitter-bonding configuration for uniform power sharing, and a package that provides for some internal matching through the use of distributed line techniques.

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SECTION I
INTRODUCTION

In order to meet the contract objective of developing a transistor with an output power of 20 watts at 2.3 gigahertz, several factors which limit the performance of transistors at higher power levels and higher frequencies were critically examined. These factors are summarized as follows:

1. A lower current gain, which necessitates modifications in the device processing in order to restore the performance at higher frequencies.
2. The intrinsic input and output impedances of the device are lowered, requiring more care in the matching networks so as to minimize the circuit losses.
3. The decrease in efficiency which requires an improvement in the thermal system to minimize the temperature rise due to the additional dissipation.
4. Package parasitics become more critical and have a greater influence on the circuitry.
5. Maintaining a uniform power distribution becomes more difficult due to a greater area and the more critical parasitics.

The developmental program was directed towards overcoming these limitations through the optimization of the device, the package, and the circuit.

SECTION II
DEVICE DEVELOPMENT

The design of a 2.3-gigahertz device capable of generating 20 watts of power output required the optimization of several interacting factors. For example, current handling capability cannot be increased without considering the effect it would have on the device parasitics (C_{ob}, C_{te}, etc.) as well as its influence on the terminal impedances. Similiarly, the thermal system produced conflicts by requiring the use of multiple-cell structures as a means of lowering the thermal resistance while maintaining a uniform power distribution to these cells. The methods used to evaluate these design trade-offs are discussed in the following paragraphs.

A. DESIGN CRITERIA

A guide to the relative power capability of devices can be determined by an evaluation of the three ratios that follow:

1. The ratio of the maximum collector current per mil of emitter periphery (I_C/EP). This ratio is a function of (a) the distribution system to the emitter-base junction (i.e., the design of the base grid, the base diffusion, and the base and emitter metallization patterns) and (b) the epitaxial collector design which determines the current at which base widening will limit power gain.

2. The ratio of the emitter periphery to the base area per cell (EP/BA). This ratio is a measure of the geometric surface configuration of the device. The emitter periphery determines the current-handling capability (along with the factors in item 1 above) and the base area determines the collector base capacitance. Therefore, a high EP/BA ratio produces a high current-handling capability at a maximum output impedance.

3. The ratio $t/(N)^{1/c}$ is indicative of the thermal resistance of the pellet, where t is the thickness of the pellet, N is the number of cells and c is the thermal-coupling coefficient and has a value between 1 and 2. A value of 1 indicates a wide cell-to-cell space and, therefore, zero thermal coupling while the value 2 indicates zero spacing (contiguous area) and a maximum degree of thermal coupling. The average capability of a device obviously is inversely proportional to this ratio.

The power design factor then becomes

$$P.D.F. = \left[\frac{I_C}{E.P.}\right] \times \left[\frac{E.P.}{B.A.}\right] \times \left[\frac{(N)^{1/c}}{t}\right]$$

This figure of merit qualitatively indicates the major design features that must be optimized in order to increase the power capability of a device. It is used, therefore, to explain the design modification used in developing the objectives of this program.

B. METAL GRID

The first factor in the P.D.F. equation (I_C/EP) requires a minimization of the voltage drop along the emitter-base distribution system, i.e., a minimum debiasing. Excessive debiasing along the emitter sites reduces the utilization of the emitter periphery and thereby reduces the effective emitter periphery. Typical values of this ratio for the mesh structure are about 1 milliampere per mil of emitter periphery. For the overlay structure, this value is approximately 2 milliamperes per mil. Values as high as 3 milliamperes per mil have been achieved with the metal-grid-overlay structure.

The metal grid replaces the p^+ silicon grid with lower resistivity platinum silicide. Thus, the metal grid reduces the resistive drop along the emitter stripe and thereby increases the current-handling capability.

The development of this new process technology is justified by the fact that it reduces the sheet resistance in the base distribution fingers from 8 ohms/square for p^+ silicon to 1 ohm/square for platinum silicide. Obviously,

such a reduction permits greater current-handling capability (I_C/EP) for a given emitter length or greater emitter lengths for a given current-handling capability. Greater emitter length results in a better design ratio (EP/BA), the second factor in the P.D.F. equation. The significant characteristics of the pellet designs which were evaluated under this contract are shown in Table I.

C. 2N6267 WITH METAL GRID

The first metal grid processing was applied to the 2N6267 pellet (Figure 1) in order to obtain an evaluation on a standard pellet configuration. These tests did result in a significant increase in current-handling capability. It was later shown, however, that this pellet was thermally limited and, therefore, the higher current-handling capability could not be utilized effectively. This thermal limitation was shown to exist by comparing low duty-pulse performance with CW operation. In this evaluation it was shown that the 2N6267 was capable of 20 watts at 2.3 gigahertz under low duty conditions; however, the power output dropped to 12 to 13 watts when the pellet was operated under CW conditions. This meant that a lower thermal resistance pellet was required.

D. TA8174

The TA8174 transistor design (Figure 2) used a multiple-cell configuration (high N in the P.D.F. equation) to lower the thermal resistance of the pellet, and a metal grid to improve the IE/EP ratio. As a result, it also had a higher design ratio (EP/BA) because it used longer emitter sites. It was felt that multiple cells with cell spacings chosen so that the thermal flux coupled in the BeO rather than in the silicon would lower the thermal resistance significantly and, therefore, raise the CW saturated power. This was later shown to be true but difficulties encountered in the development of the metal grid as well as poor power sharing between cells limited the performance of this configuration. At this point it was realized that good power sharing between cells could best be achieved by means of heavier emitter ballasting and smaller cells. Since sufficient ballasting was not possible in the TA8174, this design was abandoned in favor of one which permitted a greater degree of ballasting.

TABLE I. COMPARISON OF PELLET DESIGNS

	2N6267	TA8174	TA8641	Eight-Cell TA8407
Emitter Periphery (mils)	655	934	830	1360
Emitter Periphery To Base Area Ratio (1/Mils)	3.1	5.4	4.22	3.2
Effective Emitter Periphery To Base Area Ratio	5.6	5.4	7.35	5.7
Base Periphery (Mils)	84.2	104	162	241
Predicted θ_{jc} (^{o}C/W)	5.0	2.2	1.6	1.0
Measured θ_{jc} (^{o}C/W)	5.0	-	-	0.8-1.1
Relative Ballast Level* (MV/MV)	1.0	1.06	1.5	2.0

*Ballast level in millivolts normalized to that of the 2N6267.

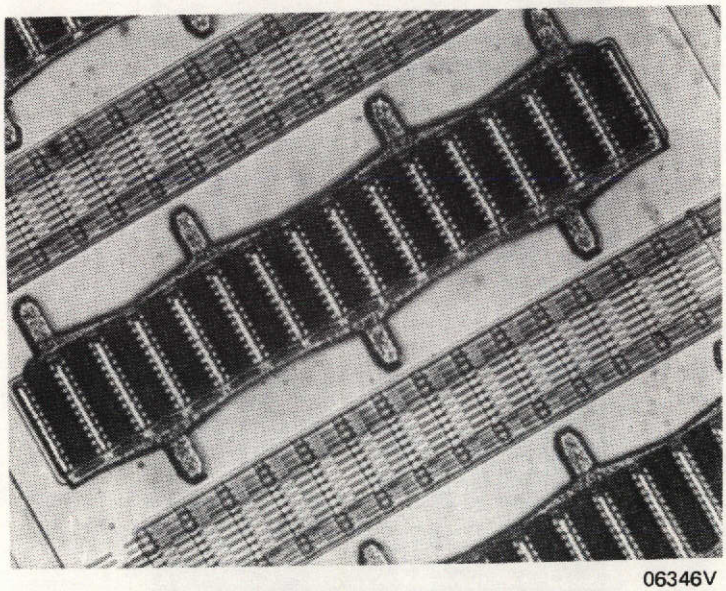

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Figure 1. 2N6267 Pellet

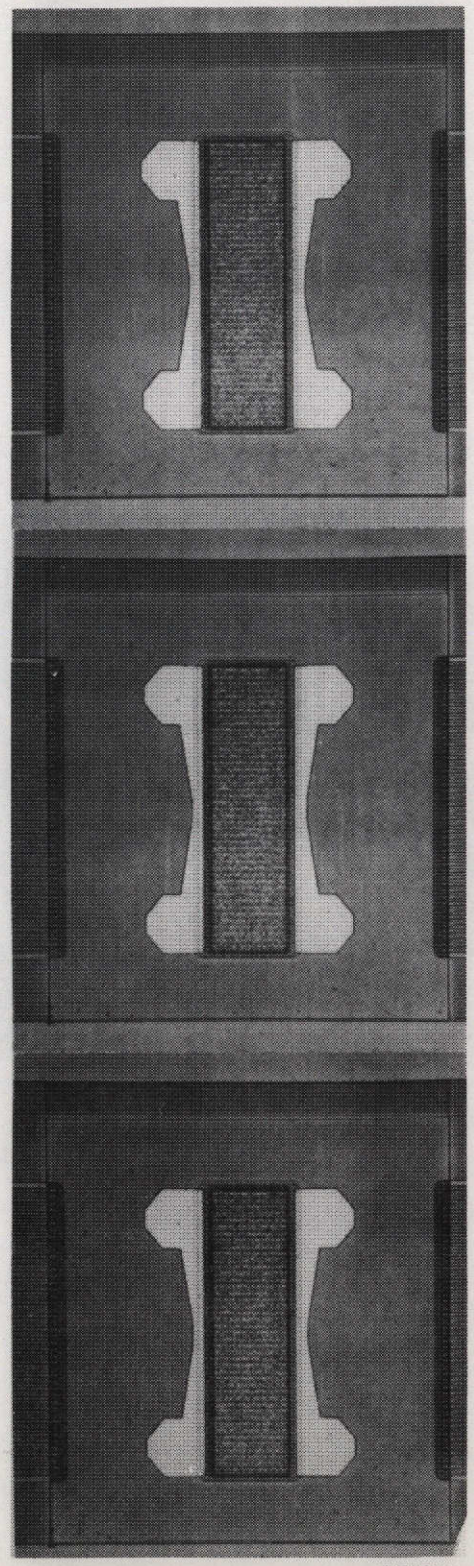

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Figure 2. TA8174 Transistor Design

E. TA8641

The TA8641 (Figure 3) was designed as a multiple-cell configuration using a metal grid with its high design-ratio capability and having the ballast capability of the standard TA8407 and 2N6267. This design is still under development but because of delays due to development difficulties in the processing of the metal-grid system, the emphasis for this project was shifted to the TA8407 device as the nucleus configuration for a multiple-cell system.

F. MULTIPLE-CELL TA8407

It was known that the single-cell TA8407 was capable of generating 2.5 watts at 2.3 gigahertz with a gain better than 9 dB. Therefore, it was felt that a multiplicity of these cells on a single pellet (see Figure 4) with design improvements would have the capability of generating 20 watts at 2.3 gigahertz.

It has often been noted that paralleling of cells can result in a significant loss of gain. Efforts concurrent with this program, however, resulted in the development of a high-frequency diffusion that provided a higher gain capability; therefore, it was felt that high gain could be maintained despite the paralleling scheme. In addition, pellet-thinning techniques developed under a thermal contract were applied to lower the thermal resistance of the system. The wide cell spacing of this pellet (11.24 mils) was also a factor in lowering thermal resistance because the lower thermal coupling reduced the value of c in the power-design-factor equation. Consequently, the thermal resistance of the TA8407 system was considerably reduced compared to the 2N6267 system (see Table I).

Power sharing between the cells was insured in two ways:

1. The configuration of the emitter bonds was found to influence the uniformity of the cell temperatures. Several configurations were tried but the simplest and most effective for this application was a slightly longer emitter bond to the end cells.

2. Heavier ballasting was required (see Table I) to insure current regulation between cells. The higher gain of the high-frequency diffusion permitted a ballasting heavier than normally used while maintaining a high gain.

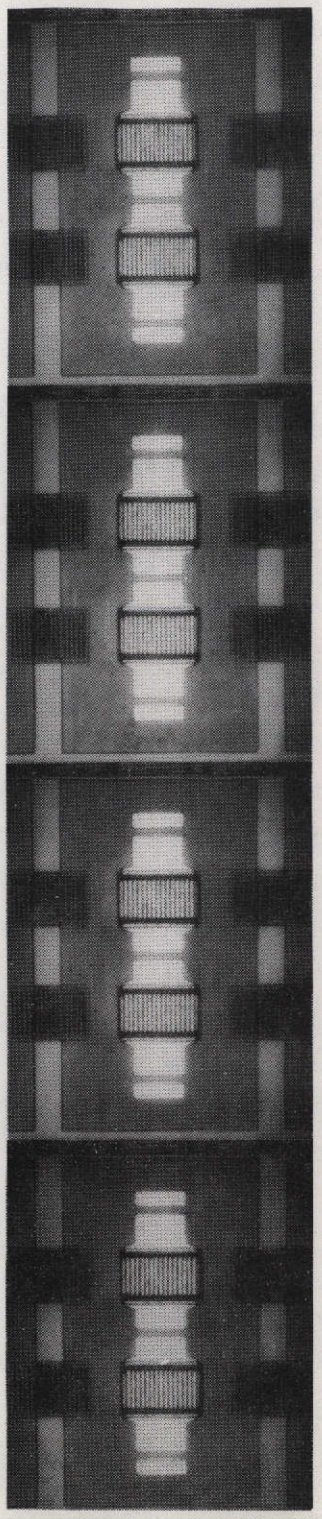

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Figure 3. TA8641 Transistor Design

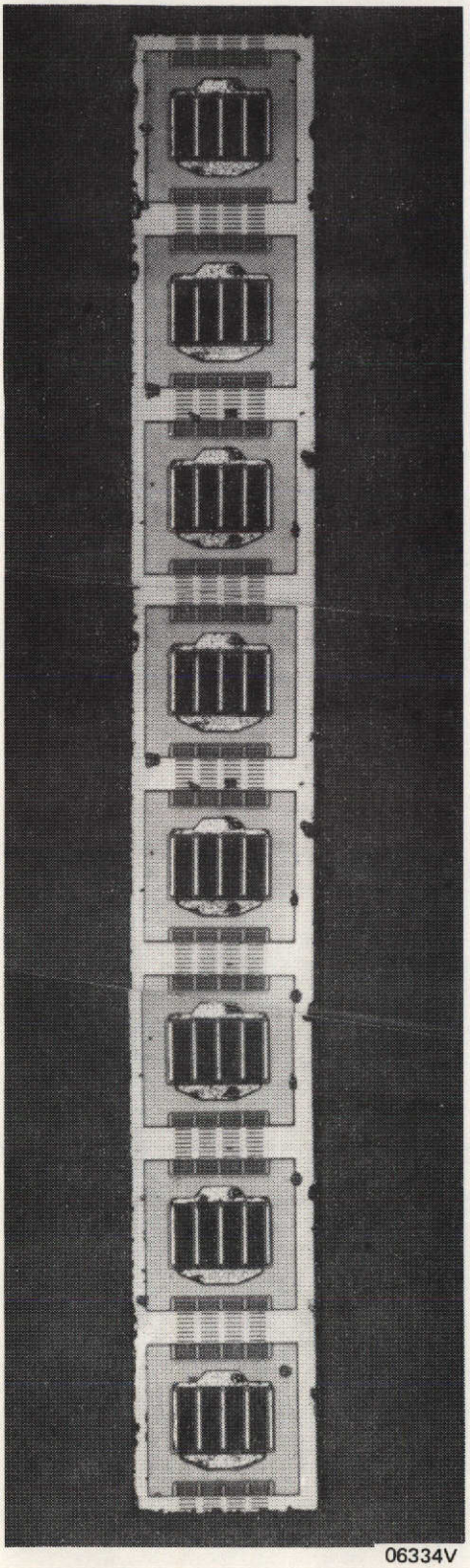


Figure 4. Eight-Cell Transistor Pellet

SECTION III
PACKAGE

The transistors were evaluated in three package configurations: the HF-28, HF-46 and a carrier/package prototype. All three are stripline devices. The initial prototypes of the chip carrier were not hermetic in order to allow the greatest degree of flexibility in choosing input and output metallization dimensions and in trimming them to optimize performance. The final package derived from the chip carrier has the same potential for hermeticity as the hermetic HF-28 and HF-46 packages. The initial prototype chip carrier is shown in Figure 5 and consists of a BeO substrate 350 by 350 by 55 mils (metallized on all surfaces) with a center collector island. In prototype package development, the input and output lines are separate pieces of Al_2O_3 and are attached to the substrate with an Au-Sn alloy. In this way there is great design flexibility, as noted above, for package optimization. Also, the final carrier design can readily be made into a hermetic package by making the input and output lines as parts of a single Al_2O_3 window as shown in Figure 6. These parts can be made "in house" with temporary tooling with a relatively short turn-around time on package development until final tooling is completed. Hermeticity is achieved by means of an additional level of Al_2O_3 above the input and output level. A cap is then brazed on this upper level.

All devices equal to or smaller than the five-cell TA8407 were evaluated in the HF-28 and HF-46 packages. The eight-cell TA8407, which is too large for these packages, was evaluated in the chip carrier. When the five-cell devices developed a maximum power output of 12 watts CW in the HF-46 package, it became obvious that eight-cell devices would be required to produce the objective 20 watts of power output. At this point, all further evaluation and optimization were done on the chip-carrier. The design of the final hermetic package followed this optimization and concluded the successful achievement of the program objectives.

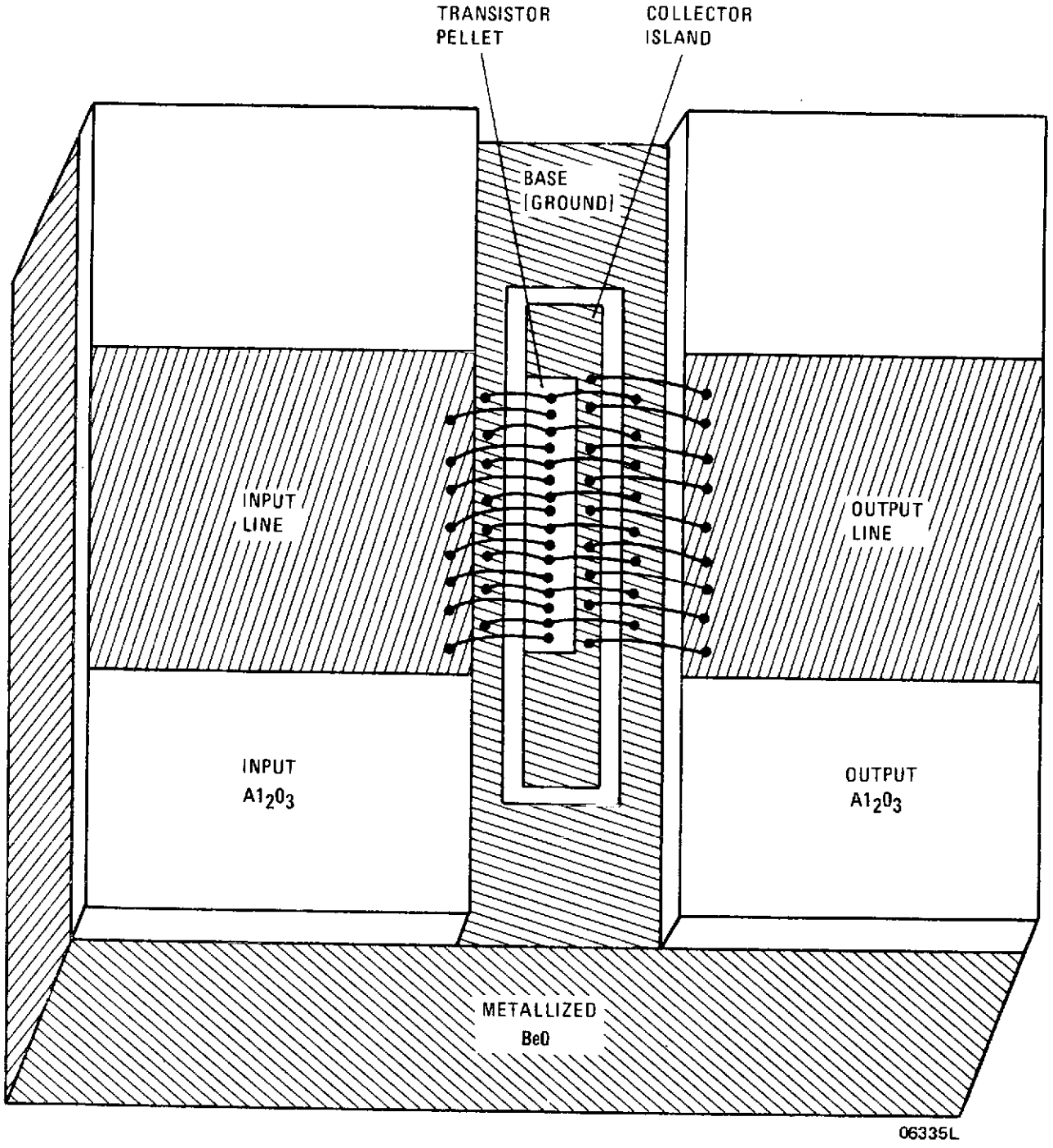


Figure 5. Carrier Used In The Development Of The Prototype Package

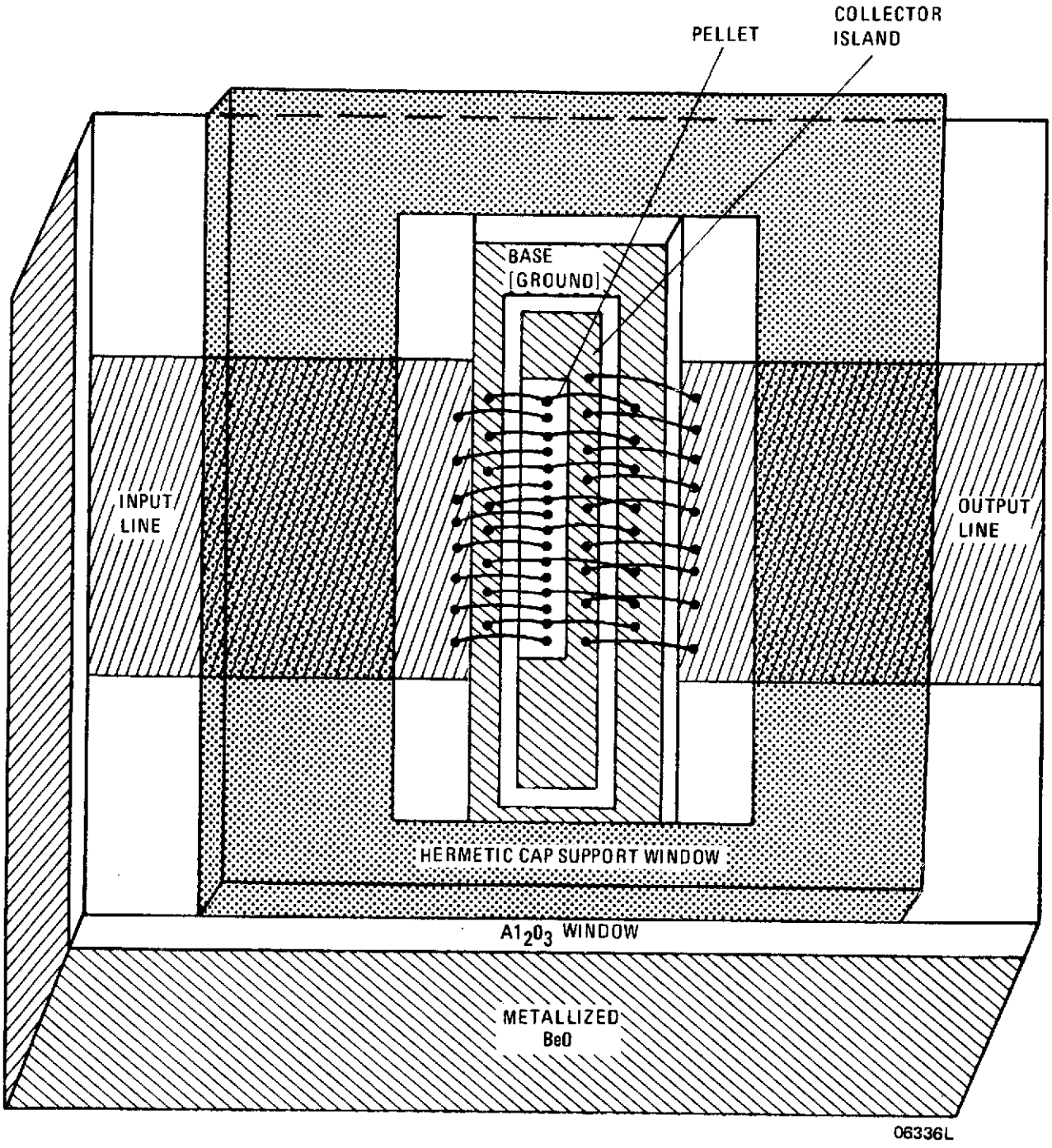


Figure 6. Continuous Al_2O_3 Window For Prototype Hermetic Package

SECTION IV
CIRCUIT DESIGN

A. GENERAL CONSIDERATIONS

The performance of discrete, microwave, power transistors is a strong function of circuit parameters as well as the generally considered device parameters. At microwave frequencies, i.e., the desired operating point of 2.3 gigahertz, the package parasitic elements of a hermetic device form a substantial part of the circuit for the device and, therefore, must be properly considered in the design of both the device and the circuit. Since hermeticity and device size requirements make it difficult to sufficiently reduce these parasitics in order to minimize their effects on the circuit, an effective microwave-power-transistor-package design must optimize the package parasitics for the transistor chip. As a first step in this package optimization a chip-carrier approach permitted the flexibility of design and the ease of design iteration required to optimize the interaction of transistor, package, and circuit. The actual physical construction of a microwave circuit, however, depends not only upon the physical and electrical characteristics of the device itself, but also upon additional characteristics, such as the desired bandwidth response, stability of response, and reliable operation at high levels of dissipation under severe environmental conditions. The test circuits should also allow for easy insertion of devices, have minimal circuit losses, and have sufficient tuning flexibility to optimize experimental device performance.

B. TEST SETUP

Because the large-signal impedance of experimental devices (or test vehicles) may vary widely during the course of a device development, the basic test setup used on this program was made as versatile as possible. Provisions were made for either forced-air or water cooling of the test fixtures and circuits because of the high dissipation levels expected for the discrete devices at the 20-watt output-power level. Pulse-test capability was also incorporated into

the test setup in order to facilitate experimental device evaluations with less risk of damage or loss during tune-up and to obtain an earlier evaluation than could be expected under CW conditions alone.

The basic test setup used on this program is shown in Figure 7. Depending upon particular test requirements, the setup could be either simplified or expanded. Calibration of the setup was performed periodically to insure accurate measurements.

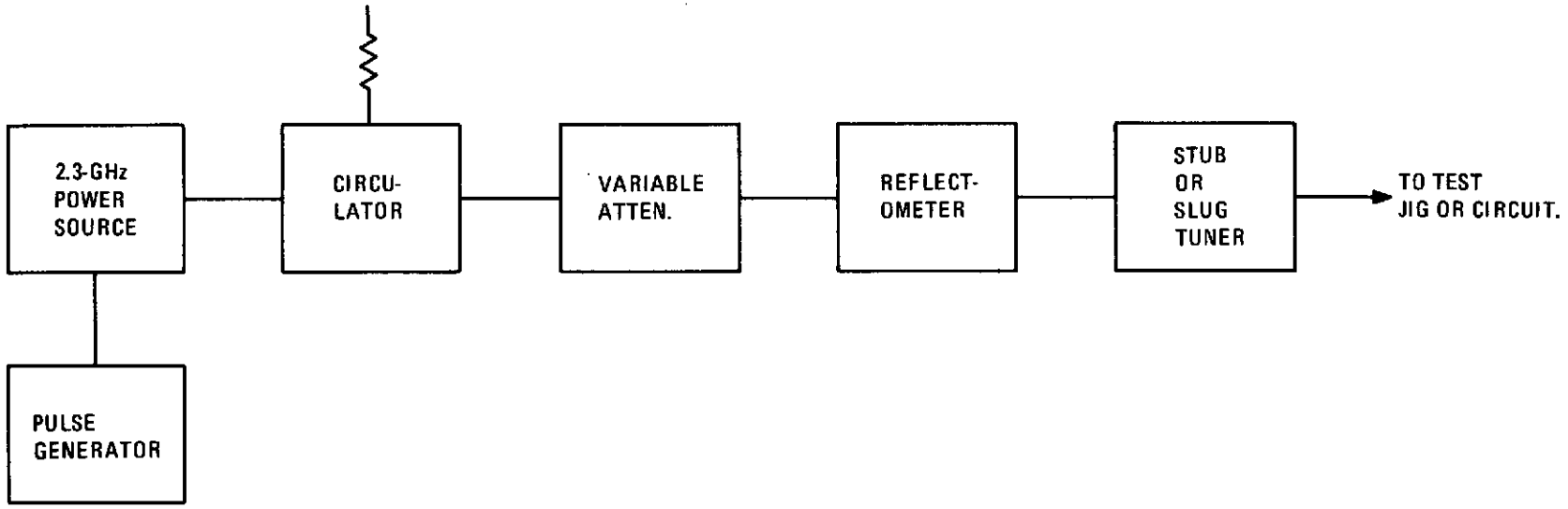
For CW measurements, input power was read on a calibration reflectometer while output power was read directly on a power bridge or calorimeter by means of an adjustable and calibrated attenuator for power-range extension. Purity of response was determined by using a spectrum analyzer coupled to the output circuit.

The test setup as shown in Figure 7 provided (at 2.3 gigahertz) calibrated input-drive levels to 4.0 watts and power-output levels up to 30 watts, which are well within the objective ranges of this program.

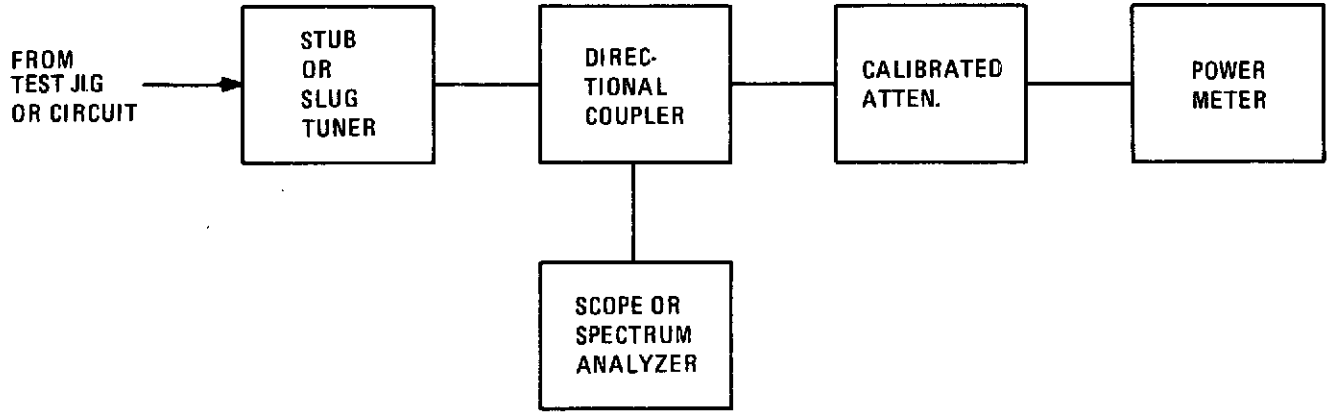
C. TEST FIXTURE DESIGNS

For the initial evaluations of new device designs under pulse conditions, simple stub-tuned test jigs were used. These jigs, which had the capability of either water or air cooling, generally required triple-stub tuners to match into the very low impedances of the developmental high-power devices. To better match into these low impedances, some simple jigs were modified by adding eight wavelength microstrip transformers at the input and output. These transformers served as first-step transformations into the device and permitted device matching with the use of lower loss, double-slug-type tuners.

New devices, packaged in existing standard RCA stripline packages, were initially evaluated in test circuits designed for evaluation of RCA standard product (such as the 2N6267). The new devices were tuned for best performance in these existing circuits alone, and then stub tuners were used to maximize the device performance. From this evaluation, new circuits were designed and constructed for final evaluation of the experimental devices; they are described in the next section of this report.



A. INPUT SECTION



B. OUTPUT SECTION

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Figure 7. Block Diagram of the Basic Test Set for Device Evaluations

Chip-carrier-type devices were also evaluated in the simple jigs to obtain initial data. Final-type carriers were also evaluated in specially designed circuits as described in the next section of this report.

SECTION V
DEVICE EVALUATIONS

A. GENERAL CONSIDERATIONS

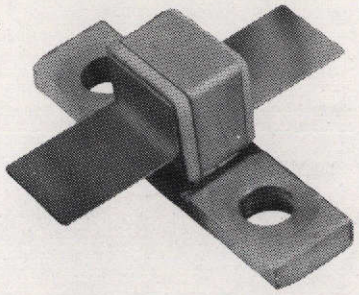
Because of the time lag experienced before a newly designed device is available for tests and evaluations, existing RCA devices were used in the initial phases of the contract to evaluate pellet design changes, circuit design approaches, and test setups. The information obtained from these interim evaluations was utilized in the final-device and circuit designs to obtain the desired objective performance of the program.

B. EVALUATION OF THE 2N6267 DEVICE

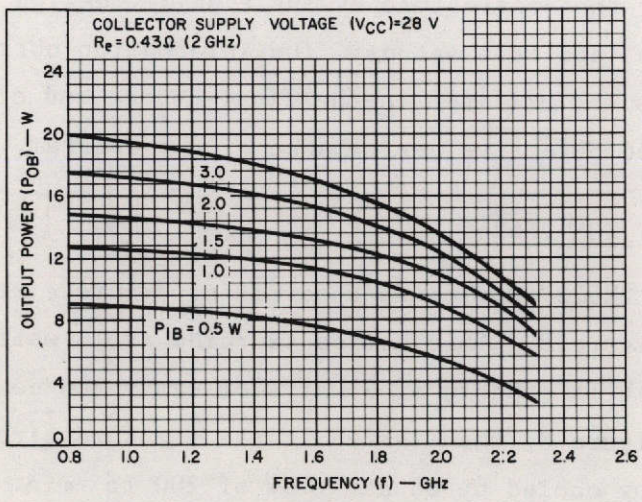
The RCA type 2N6267 device is a hermetic, discrete stripline device packaged as shown in A, Figure 8. This device is rated at 10 watts with 10-dB gain at 2.0 gigahertz. It is capable of 9 watts of saturated power at 2.3 gigahertz, as shown in B, Figure 8, when tested in the standard circuit of C, Figure 8 with the jig being cooled by an air flow of 200 ft^3/min.

Selected 2N6267 devices, including some metal-grid versions, were evaluated in circuits optimized for performance at 2.3 gigahertz. A simple lumped-constant circuit which utilizes the device and package parameters in an L-network to transform the device impedances directly to 50 ohms is shown in A, Figure 9. While this circuit indicated good potential performance for the 2N6267 devices, isolation between input and output was inadequate and, thus, tuning was critical.

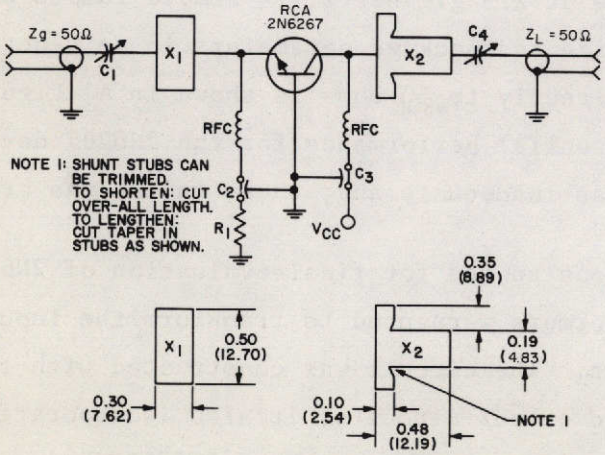
The circuit of B, Figure 9 was constructed for final evaluation of 2N6267 devices. Simple tapered-line transformers were used to transform the input and output impedances directly to 50 ohms. The circuit was constructed with complete shielding between the input and output circuits; it also incorporated water-cooling capability. Typical performance for selected 2N6267 devices in this circuit is shown in Figure 10. Typical devices developed about 11 watts under CW conditions but about 14 to 15 watts under 50-percent pulse (1-kilo-



A. 2N6267 Device in the HF 28 Package



B. Typical 2N6267 Performance



Dielectric material: 1/32 in. (0.79 mm) thick Teflon-fiberglass double-clad circuit board (ϵ = 2.6). Lines X_1 and X_2 are produced by removing upper copper layer to dimensions shown.

C. Typical 2.3-Gigahertz Circuit

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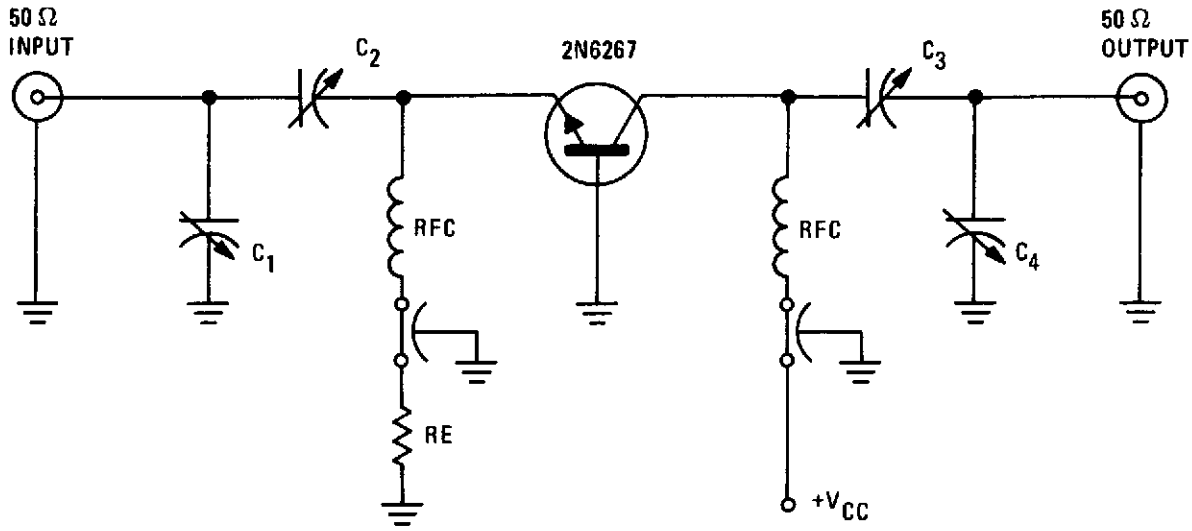
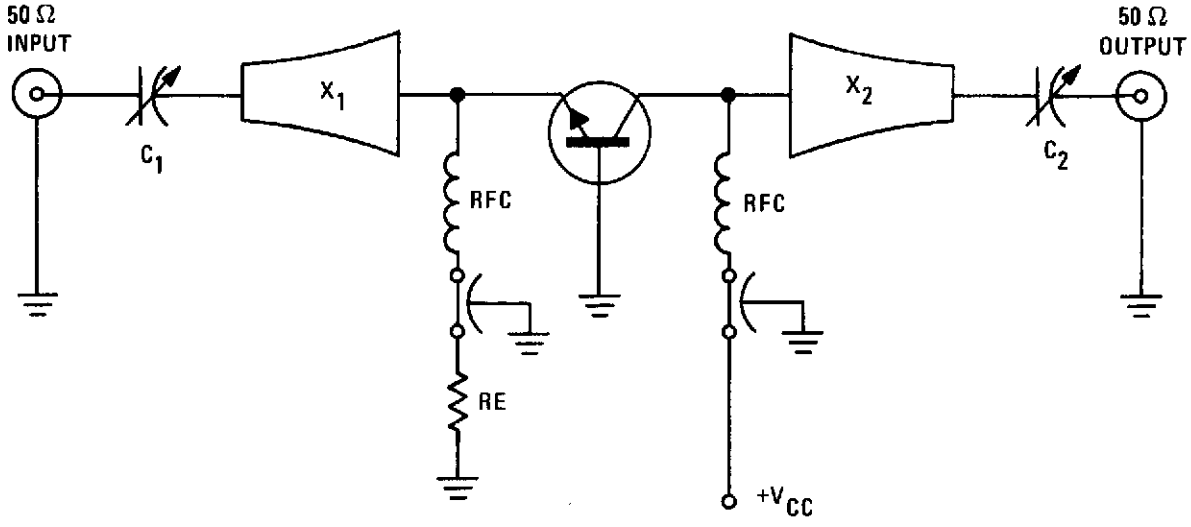
Figure 8. Rated Performance of the 2N6267 Device



C_1, C_2, C_3, C_4: 0.3-3.5pF JOHANSON

A. SIMPLE L-NETWORK CIRCUIT



C_1, C_2: 0.3-3.5 pF JOHANSON

B. SIMPLE MICROSTRIP CIRCUIT

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Figure 9. Final Design Circuits for Evaluation of 2N6267 Devices

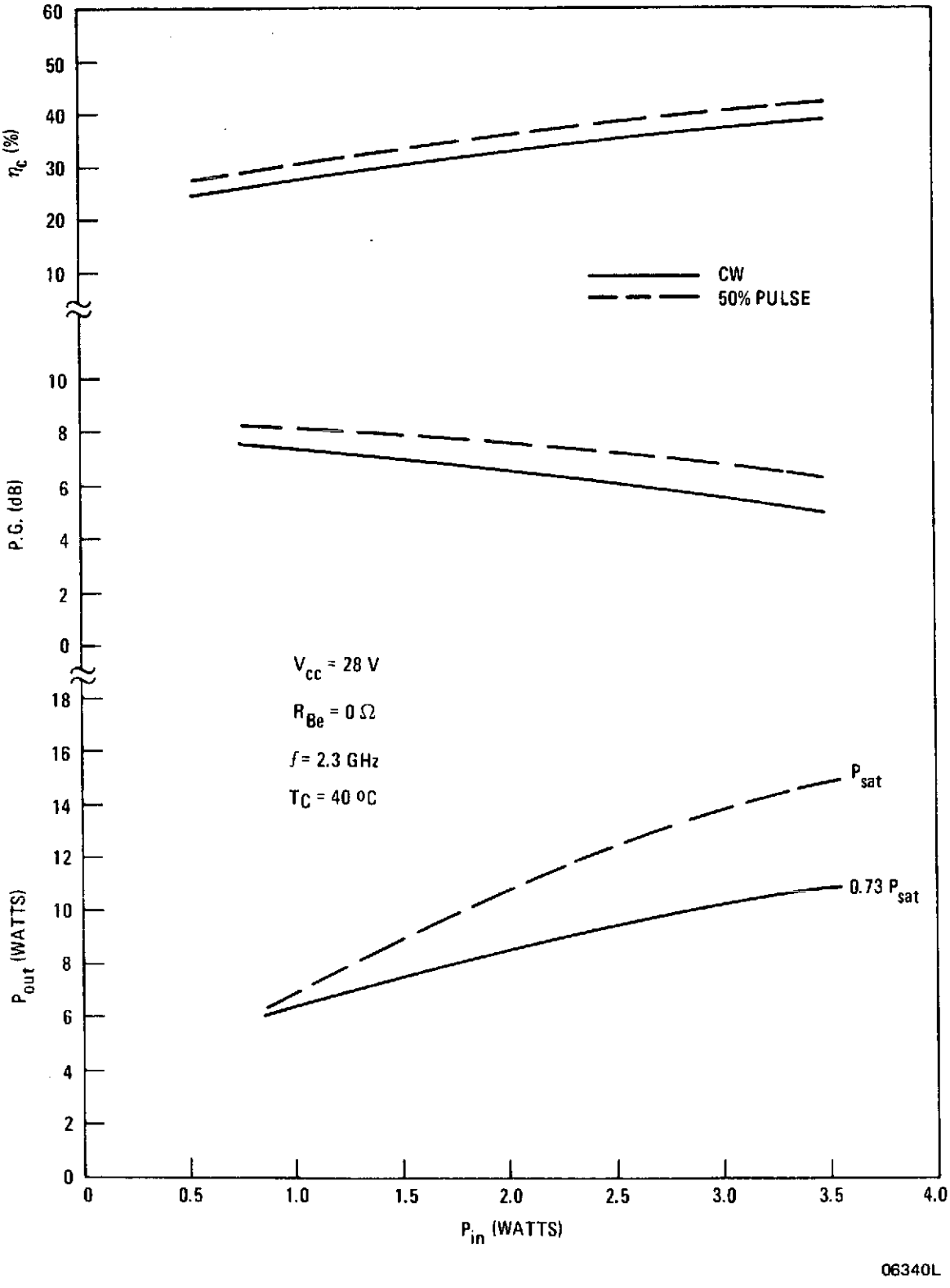


Figure 10. Typical Performance of the 2N6267 in a Shielded Circuit

hertz rate) conditions. The best units were able to develop about 12 to 13 watts under CW conditions and 16 to 17 watts under 50-percent pulse conditions. It was apparent that some sort of pellet and or package thermal limitations were present in these devices. Since the 2N6267 pellet is a large integral pellet with strong thermal coupling between pellet sections, it was decided to continue further tests on a multiple-cell configuration. The multiple-cell configuration allowed improved thermal isolation, the possibility of isolated matching networks, and improved power sharing between cells. Evaluations were made in a revised microstrip-package design as well as in chip-carrier-type-package designs.

C. MULTI-CELL EVALUATIONS IN THE HF-46 PACKAGE

Preliminary evaluations had indicated that thinned-down type TA8407 pellets having a higher frequency diffusion had a much improved CW performance over standard product at 2.3 gigahertz. To simplify the evaluation of multi-cell devices based upon this modified type TA8407 unit cell, the RCA HF-46 stripline package was used. This package could be used without the final cap seal used for hermetic sealing, and thus facilitated bonding tests for the various ex-mental devices. Both infrared temperature measurements and RF evaluations had indicated the importance of the ratio of the bonding wire sizes and configurations to the overall performance of the various experimental devices (as discussed in the design section of this report).

RF evaluations of experimental multi-cell devices in the HF-46 package were made in simple test jigs under pulse conditions. Performance under CW conditions were made in a circuit similar to that shown in C, Figure 8. Stub tuners were used to optimize the performance of the various device configurations.

The HF-46 package could accommodate a maximum of five cells of the high-performance TA8407 pellet. In order to develop maximum power, therefore, five-cell devices were mainly used in these evaluations. The best performance was obtained from shallow-diffused pellets having "fanned" emitter lead bonds that were "double-stitched" with 1.2-mil bond wire. The input bonding configuration appeared to be related to both the common-base feedback effects and the input

parasitic capacitances. The collector bond configuration (e.g., primarily the number and diameter of collector wires) was found to effect efficiency largely, while the input bonding configuration had first-order effects on current sharing between cells (as indicated by cell-temperature response in infrared measurements).

The best performance achieved from an optimized five-cell device in the HF-46 package is shown in Figure 11. Both 50-percent (1 kilohertz) and CW performance are plotted. As can be seen now, the power spread between pulse and CW operation is not as severe as it was in the case of the 2N6267 pellet as shown in Figure 10. At the 2-watt drive level, the five-cell TA8407 device had had much more improvement in power, power gain and efficiency than could be accounted for with about a 20-percent increase in pellet size (compared to the 2N6267). This improvement can be related to the higher frequency diffusion and to the improved thermal response and current sharing that was noted with the multi-cell approach used in this HF-46 package.

Since only about 15 watts of saturated power could be expected with the five-cell (maximum) device in the HF-46 package, a chip-carrier-type package, which would be capable of handling up to 10 cells, was designed for further evaluations in order to achieve the desired 20-watt power output required by this program.

D. EVALUATION OF THE CHIP CARRIER HAVING ISOLATED INPUT MATCHING

To facilitate experimental evaluations, chip-carrier-type tests were made on a common 0.350 inch by 0.350 inch by 0.055 inch block of beryllia (see Figure 5). Appropriate metallizing patterns and alumina input and output lines could be constructed on these blocks and the carrier could be evaluated in common test jigs or circuits. Double-stitching of the base leads to the carrier ground planes (or one lead to a base bridge) could be achieved as could multiple bonding between the collector island and the output line (see Figure 5). Input bond lengths and wire sizes could be used to adjust the input-lead inductance values.

The input matching investigated on this program related only to the first-step transformation seen in an L-network which is provided by the bonding-wire configuration and an MOS capacitance as shown in A, Figure 12. As seen here,

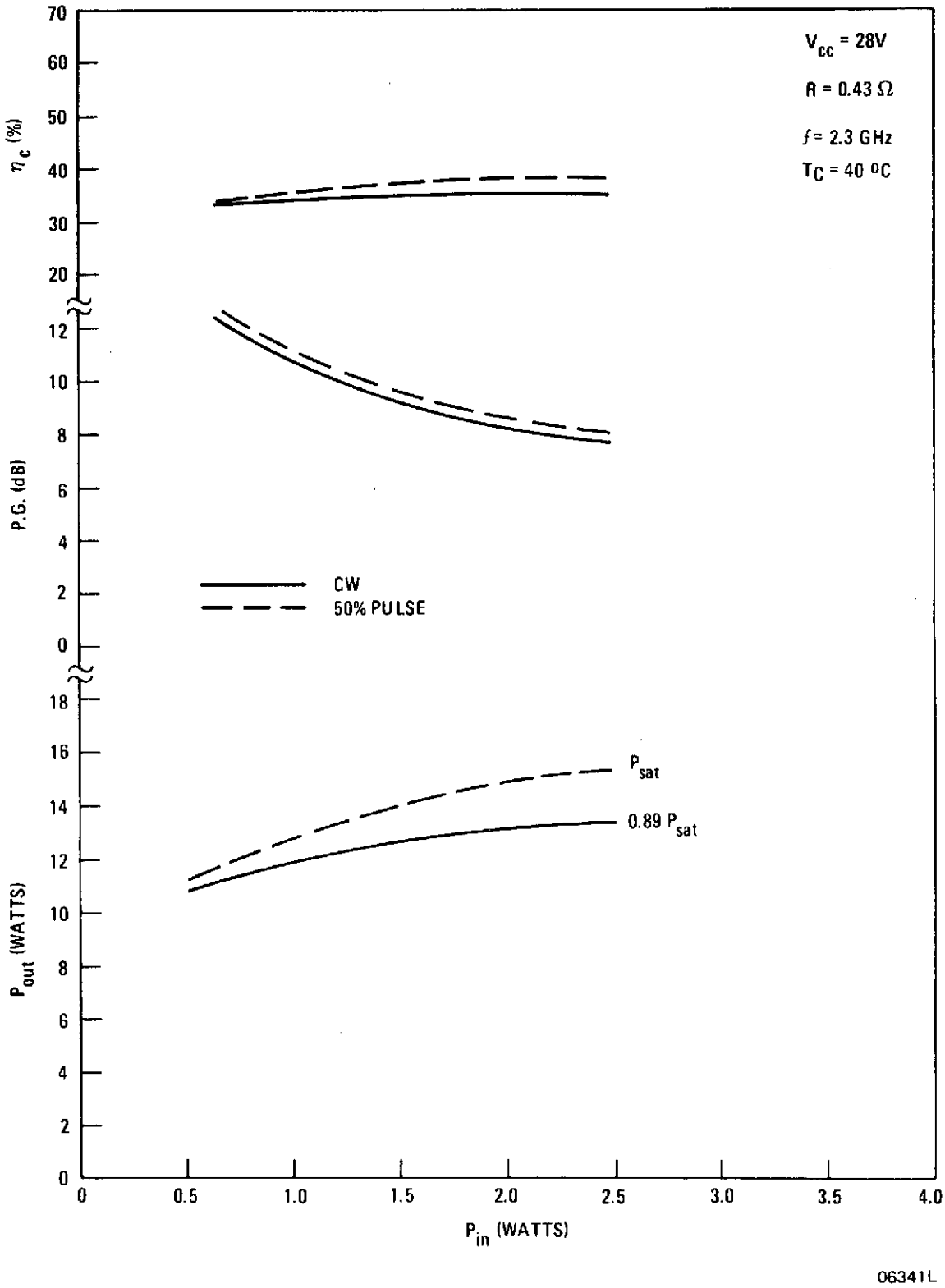
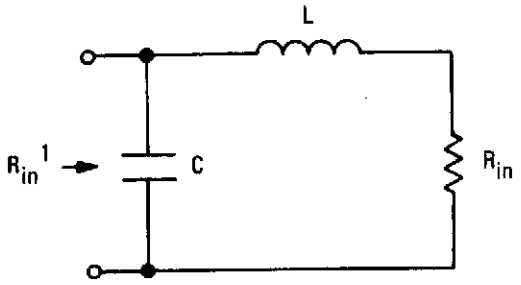


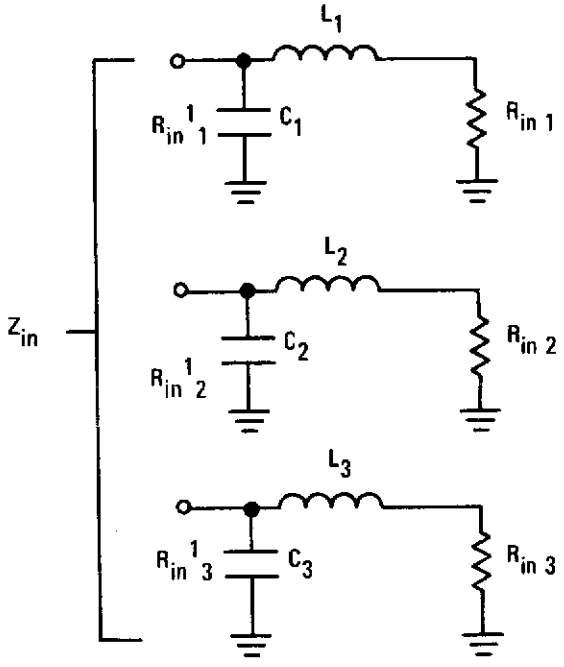
Figure 11. Performance of the Five-Cell TA8407 in a Shielded Circuit (HF-46 Package)



$$X_L = \sqrt{R_{in}\,R_{in}{}^{1} - R_{in}{}^{2}}$$

$$X_C = \frac{R_{in}\,R_{in}{}^{1}}{X_L}$$

A. L-NETWORK REQUIREMENTS FOR A RESISTIVE IMPEDANCE MATCH



$$R_{in\,1} = R_{in\,2} = R_{in\,3}$$

$$L_1 = L_2 = L_3$$

$$C_1 = C_2 = C_3$$

$$R_{in}{}^{1}{}_{1} = R_{in}{}^{1}{}_{2} = R_{in}{}^{1}{}_{3}$$

$$Z_{in} = \frac{R_{in}{}^{1}}{3}$$

B. ISOLATED L-NETWORK IN A THREE-CELL STRUCTURE UNDER RESISTIVE MATCH CONDITIONS

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Figure 12. Matching With Isolated Input L-Networks

the real device impedance, $R_{in'}$, is transformed to a new real impedance, R_{in}, only when the specified conditions are met. In most discrete packages, capacitance C is controlled by the package requirements, and inductance L may be highly limited in useful range. Thus, discrete packages generally have an upper limit of usefulness (unless carrier concepts are used in their design), even though a high-frequency-performance pellet may be available.

When multiple cells are to be combined in a simple parallel combination, it is important that these L-networks transform the common (paralleled) input resistance to the correct R_{in} at each cell for proper current sharing between cells, as shown in B, Figure 12 for the isolated-input case. If all elements of this system are equal, but are not necessarily resonant, the input drive would be reactive, but the R_{in}'s would still be equal, i.e., the cells would share the available power equally. If for any reason any reactive term should change, then a compensatory change in the other reactive term of the L-network must be made to keep the power division equal. By using MOS capacitors for capacitance C, the isolated-input approach is feasible with simple L-networks because C can now be defined correctly for each application.

An initial test of this approach was made with a four-cell TA8407 carrier where the MOS capacitance per transistor cell was 22 picofarads and L was in the order of 0.85 nanohenry. This network was resonant at about 1.6 gigahertz, and achieved a performance of 12 watts of output power (50 percent pulsed) with a power gain of 8 dB and a collector efficiency of 45 percent. Performance remained good below 1.6 gigahertz but fell off above 1.6 gigahertz due to the low-pass nature of this L-network.

A six-cell TA8407 carrier was assembled in which each pair of cells was paralleled to one 22-picofarad MOS capacitor. Perforamnce was now extended to 1.9 gigahertz where 15 watts of output power (50 percent pulsed) with a power gain of 10 dB and a collector efficiency of 36 percent was now obtainable. Again, the roll-off of the low-pass filter characteristics was noted above this frequency.

Finally, a six-cell TA8407 carrier was assembled in which each pair of cells were paralleled to a 12-picofarad MOS capacitor. Performance was now extended to about 2.2 gigahertz where 12 watts of output power (50 percent pulse)

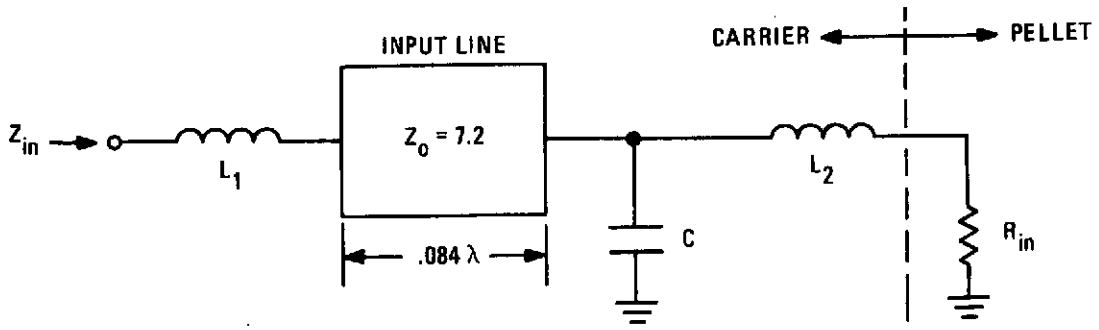
with a power gain of 11 dB and a collector efficiency of 32 percent was now available. Again, good performance was noted below this resonance point, while a sharp fall-off was seen above it. It became clear that the development of high power output by means of multiple-cell structures required only the assurance that: (1) cells receive their proper share of the available input power through uniform first-step transformations, (2) cells are adequately thermally isolated and adequately coupled to the external heat sink, and (3) that the first-step transformation, i.e., the internal L-network to each cell, operates at either the resistive resonant point or below it.

These concepts were generally pursued in the optimization of the final carrier. It was found, however, that the isolated network was not required to achieve good power sharing because the increase in the level of site ballasting (see Table I) and the optimization of the bonding configuration produced the required power sharing without adding the complexity of the isolated input networks.

E. EVALUATIONS OF FINAL CHIP-CARRIER DESIGNS

Previous evaluations had indicated that it was possible to obtain at 2.3 gigahertz about 3.0 to 3.5 watts of saturated power per cell from the high-performance-type TA8407 device. It was estimated that due to thermal coupling, an eight-cell TA8407 would only develop between 2.5 and 2.75 watts of saturated power per cell. Therefore, 20 watts of output power was considered feasible with an eight-cell structure.

The device input and output impedances were calculated. These calculations were based upon the eight-cell geometry used in the final design. The input and output lines of the carrier were chosen with characteristic impedances (Z_o) approximately equal to the magnitude of the initially calculated device impedances. Input bonding positions were chosen with relation to fringe field effects on the input line. A maximum number of collector bonds were utilized to minimize this inductance and also to interweave with base bonds so as to minimize capacitive feedback effects. The calculated parameters, which were based upon the final-design-carrier dimensions and geometry, are given in Figure 13. The input and output impedances include the effects of the lead in-



L_1 ≅ 0.25 nH "CONNECTION"

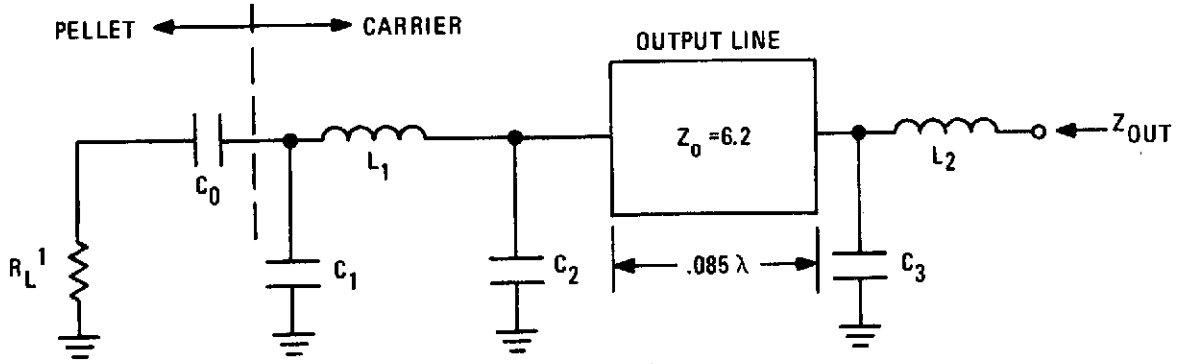
L_2 ≅ 0.25 nH, EFFECTIVE BOND INDUCTANCE

C ≅ 1.6 pF, EFFECTIVE "FRINGE" FIELD OF INPUT LINE

R_{in} ≅ EFFECTIVE PELLET IMPEDANCE

Z_{in} ≅ 1 + j 3.8 Ω (MEASURED)

A. INPUT MODEL



$R_L{}^1$ ≅ 1.4 Ω

C_0 ≅ 18 pF

C_1 ≅ 0.5 pF, COLLECTOR PAD "FRINGE" CAPACITANCE

C_2, C_3 ≅ 1.6 pF, OUTPUT LINE "FRINGE" CAPACITANCE

L_1 ≅ 1.25 nH, EFFECTIVE COLLECTOR BOND INDUCTANCE

L_2 ≅ .12 nH, EFFECTIVE OUTPUT "CONNECTION"

Z_{OUT} ≅ 2.1 + j 5.1 Ω (CALCULATED)

≅ 1.9 + j 5.1 Ω (MEASURED)

B. OUTPUT MODEL

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Figure 13. Simplified Model for the Final Eight-Cell TA8407 Chip-Carrier Design

ductance used to make a connection to the circuit. As shown by the sample models in Figure 13, close agreement was achieved between measured and calculated impedances.

Using the initially calculated impedances as a basis, a fully-shielded circuit was constructed as shown in Figure 14. This circuit is shown schematically in Figure 15. Two degrees of tuning were incorporated into the input and output networks in order to match small-range impedance variations. The output circuit matches 15- to 20-watt devices very well; however, because the input circuit was designed for higher impedance values than were achieved in the final design, it requires some further adjustment in the length of the input-line section. The final chip-carrier devices, however, were evaluated with the circuit optimized for one stub-tuned device. These were then used for the remaining device-to-device evaluations.

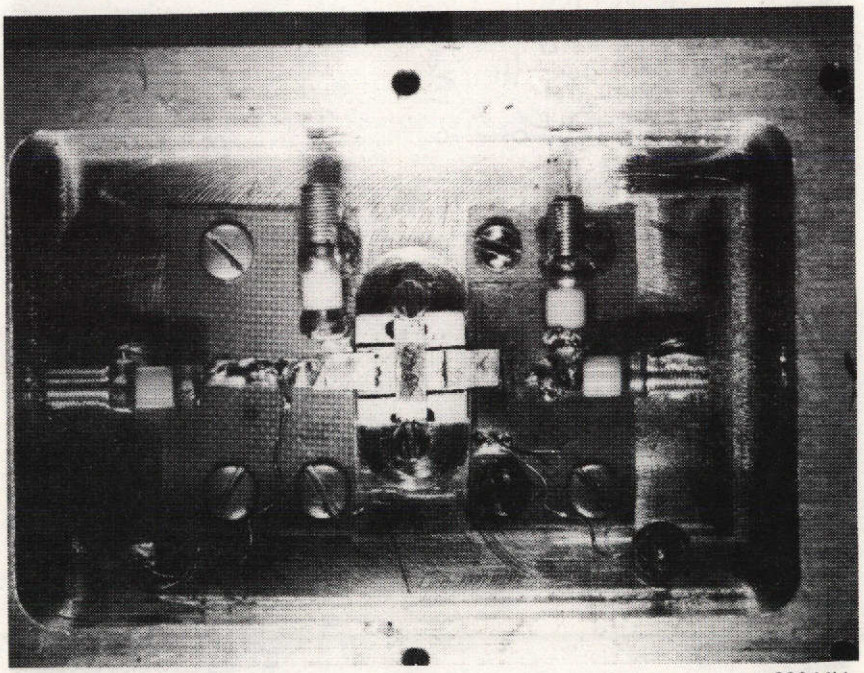

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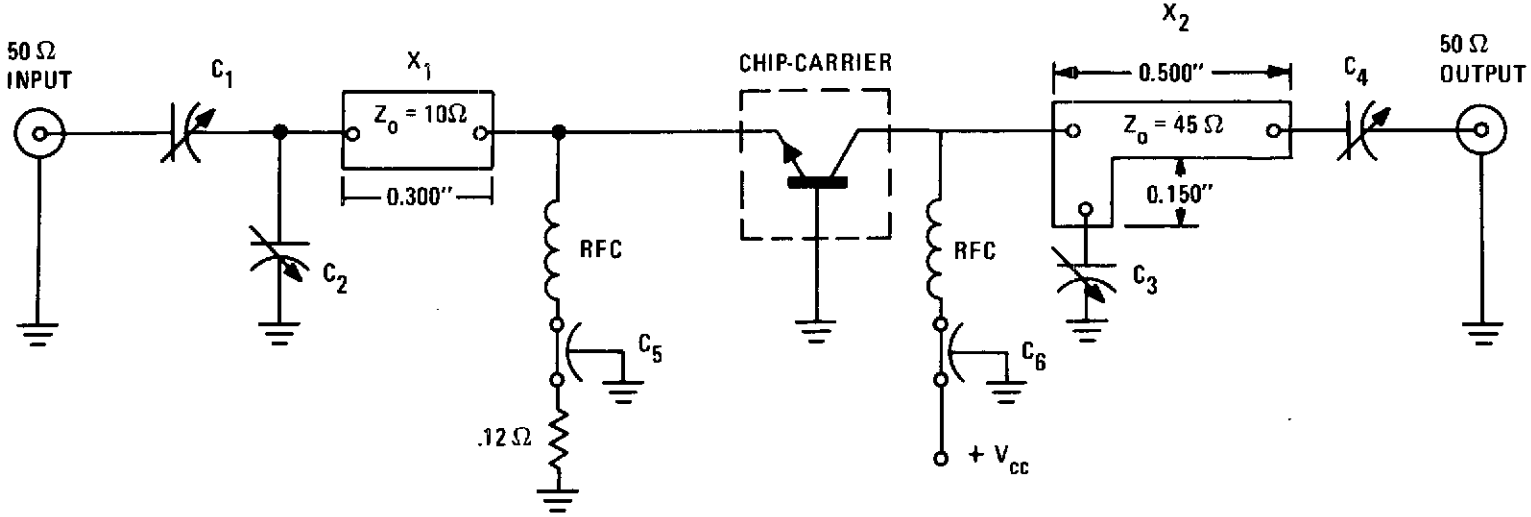
Figure 14. 2.3-Gigahertz Microstrip Circuit



X_1, X_2: FABRICATED ON 1/32" TEFLON-FIBERGLASS BOARD

C_1, C_2, C_3, C_4: 0.3-3.5 pF JOHANSON TYPE CAPACITOR

C_5, C_6: A-3 FILTERCON TYPE CAPACITOR

RFC: 0.10 μH CHOKE

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Figure 15. 2.3-Gigahertz Microstrip Circuit For Use With Final Design Chip-Carrier Units

SECTION VI
CONCLUSIONS

A CW power output of 23 watts was achieved at 2.3 gigahertz with a power gain of 7.7 dB and an efficiency of 40 percent at a case temperature of 70°C. This performance was achieved with eight cells of the basic TA8407 pellet design configuration but with modifications in the pellet processing and package design which raised the frequency and power capability of the RF system.

Through the use of a high-frequency diffusion, the power gain performance of the pellet was raised significantly. In addition, the average power capability was increased by means of a better thermal design, i.e., thinner pellets and multiple cells. Power sharing between cells was achieved by using heavier emitter-site ballasting and by the optimization of the emitter-bond configuration.

Performance data on delivered samples are given in Appendix A.

APPENDIX A
DELIVERIES AND PERFORMANCE DATA

Twenty-five devices have been fabricated for delivery. The first five consist of the modified eight-cell TA8407 mounted on chip carriers. The performance of these units is shown in Table II. Twenty additional units were fabricated in packages of the final-design configuration shown in Figure 6. The performance of these units is given in Table III.

TABLE II. CW PERFORMANCE OF THE CHIP-CARRIER FINAL SAMPLES AT 2.3 GIGAHERTZ

Sample No.	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)	Gain (dB)
1	1.0	18.0	35	12.5
	1.5	19.2	37	11.1
	2.0*	20.0	39	10.0
2	1.0	15.5	32.2	11.9
	1.5	16.8	34.5	10.5
	2.0	17.8	35.2	9.5
	2.5	18.6	36.0	8.7
	3.0*	19.1	36.0	8.1
3	1.0	16.0	34.0	12.0
	1.5	17.0	36.0	10.5
	2.0*	17.5	36.0	9.4
4	1.0	15.8	32.2	12.0
	1.5	17.0	34.0	10.5
	2.0*	18.0	36.0	9.5
5	1.0	14.8	32.0	11.7
	1.5	16.2	33.6	10.3
	2.0	17.2	34.2	9.3
	2.5	17.7	34.5	8.6

Conditions: V_{CC} = 28 V; R_{be} = 0.12 ohm;
T_{case} = 40°C

*Saturation level

TABLE III. CW PERFORMANCE AT 2.3 GIGAHERTZ OF THE 20 PACKAGED FINAL SAMPLES

Sample No.	Device No.	P_{IN} (W)	P_{OUT} (W)	I_C (A)	Efficiency (%)	Gain (dB)
1	1	4.0	22.5	2.1	38	7.5
2	2	4.0	22.0	1.95	40	7.4
3	3	4.0	21.5	2.0	38.4	7.3
4	4	4.0	22.0	2.0	39.3	7.4
5	6	4.0	23.0	2.1	39.1	7.6
6	7	4.0	21.0	1.9	39.3	7.2
7	8	4.0	22.5	2.05	39.3	7.5
8	9	4.0	23.5	2.1	40.0	7.7
9	11	4.0	22.5	2.05	39.0	7.5
10	12	4.0	21.0	2.0	37.5	7.2
11	15	4.0	19.8	1.9	37.0	6.9
12	18	4.0	18.8	1.8	37.1	6.7
13	20	4.0	19.8	1.8	39.0	6.9
14	21	4.0	21.0	1.9	39.4	7.2
15	22	4.0	20.4	1.9	38.4	7.1
16	23	4.0	19.8	1.85	38.0	6.9
17	24	4.0	19.8	1.8	39.1	6.9
18	25	4.0	20.4	2.0	36.4	7.1
19	26	4.0	19.8	2.0	35.3	6.9
20	27	4.0	21.0	1.9	39.3	7.2

Conditions: V_{CC} 28 V; R_e = 0.12 ohm;
T_{case} = 70°C